REMARKS/ARGUMENTS

In paragraph 5 of the Office action, claims 1-29, 31-34, 36-42 and 44 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Hariguchi et al. U.S. Patent No. 6,665,297 ("Hariguchi"). It is respectfully submitted that the Examiner reads too much into the Hariguchi patent and has overlooked elements in the pending claims which clearly define over Hariguchi.

With respect to independent claim 1, the Examiner cites Figures 3-4 and 7 of Hariguchi for the limitation "enabling portions of a CAM in response to the hash signals." There is nothing in the figures cited by the Examiner to indicate that portions of the CAM are enabled in response to the hash signals. In contrast, the hash signals are input to a hash bucket stage, the output of which is input to a selection stage. As seen in Figure 3, the CAM has a plurality of masks associated with stored addresses. The destination address is input to each of the masks such that it is apparent that the entire CAM is enabled. Thus, it is applicant's position that the Office has not demonstrated that Hariguchi discloses "enabling portions of a CAM in response to said hash signals." Because the Office has not demonstrated that Hariguchi teaches that element, it follows that the element of "comparing said input word in the enabled portions of said CAM" has also not been demonstrated as being taught by Hariguchi. For those reasons, it is respectfully submitted that claims 1 is patentable over Hariguchi.

With respect to claim 8, as set forth in paragraph 7 of the Office action, the Office cites Figure 7 as disclosing the limitation "pre-charging certain portions of a CAM in response to said hashing step". As disclosed in paragraph 7 of the application as originally filed:

> FIG. 6 shows a typical CAM row 10 as having n CAM cells 12(l)-12(n) each coupled to an associated match line ML. A pull-up transistor 14, coupled between a supply voltage VDD and match line ML, has a gate tied to ground potential, and therefore remains in a conductive state. Prior to each compare operation between an n-bit comparand word and an n-bit CAM word stored in CAM cells 12(l)-12(n), match line ML is pre-charged to supply voltage VDD via pull-up transistor 14. The n-bits of the comparand word are compared with corresponding bits of the CAM word in respective CAM cells 12(l)-12(n). If all bits of the comparand word match corresponding bits of the CAM word, the match line ML remains charged to indicate a match condition. Conversely, if one of the comparand bits does not match the corresponding CAM bit, the CAM cell 12 storing that CAM bit discharges match line ML toward ground potential to indicate a mismatch condition.

Turning to Figure 7 of Hariguchi, element 206 recites generating a hit/miss signal for each hash circuit and for the CAM. Thus, there is one hit/miss signal generated for the entire CAM. This is apparent from the previous step 204, which indicates that the IP destination address is input to the CAM. Although Figure 7 says nothing about pre-charging of the CAM, it seems logical that for one hit/miss signal to be generated for the entire CAM, the entire CAM is pre-charged. It is therefore believed that Hariguchi is operating according to the prior art in which the entire CAM is pre-charged. Thus, the benefit of the present invention, pre-charging only those portions of the CAM in which a match is likely to occur, is not suggested by Hariguchi.

In paragraph 8 of the Office action, independent claim 15 is rejected on the basis of Hariguchi. The Examiner cites Figures 2A and 2B of Hariguchi as disclosing "using the hash signals to identify portions of a CAM" and as disclosing "comparing the address in only the identified portions of the CAM". As seen in Figures 2A and 2B, the outputs of the hash circuits are input to the selection stage, not the content addressable memory 80. The hash signals of Hariguchi do not identify portions of a CAM such that a comparison of the address occurs in only the identified portions of the CAM. For those reasons, it is respectfully requested that the rejection of claim 15 be withdrawn.

Claim 22 recites "pre-charging certain portions of a CAM in response to said hashing step" and "comparing said internet address in said pre-charged portions of the CAM". For the reasons set forth above, it is respectfully suggested that claim 22 is in condition for allowance as the recited steps have not been demonstrated as being taught Hariguchi.

In claim 28, a circuit is recited which comprises "a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word" and "a circuit, responsive to said hash signals, for pre-charging portions of said CAM". In paragraph 10, the Examiner cites column 4, line 31 through column 5, line 63 as disclosing a circuit for pre-charging portions of the CAM. In column 5, beginning at line 15, it is disclosed that the inputs of the hash circuits 82 of the hash table 70 are connected in parallel with inputs of the CAM 80. This is clearly seen in Figures 2A and 2B. The circuit responsive to the hash signals in Figures 2A and 2B is the selection stage 88. It is not seen in Figures 2A and 2B how this selection stage 88 is used to pre-charge portions of CAM 80 in response to the hash signals. Thus, it is respectfully requested that the rejection of claim 28 be withdrawn.

Claim 34 recites enable logic, responsive to said plurality of memory devices, for enabling portions of said CAM. The memory devices are recited as being "responsive to said hash circuits". Thus, the enable logic is ultimately responsive to the plurality of hash circuits for enabling portions of said CAM. As has already been described, Hariguchi has not been demonstrated as disclosing enabling portions of the CAM in response to the hash circuits. Thus, it is respectfully requested that the rejection of claim 34 be withdrawn.

Claims 39 and 40 have been cancelled.

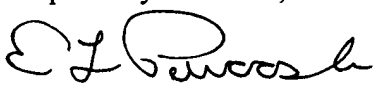
With respect to claim 41, the Examiner cites column 3, lines 8-20 of Hariguchi as teaching calculating bank run length information. The cited portion of Hariguchi discusses U.S. Patent No. 5,386,413 ("the 413 patent"). As seen from Figure 5 of the '413 patent, each mask circuit has its own memory array 130, 131 or 132. It is not seen how the cited portion of Hariguchi teaches "calculating bank run length information". Accordingly, it is Applicant's position that the Office has failed to demonstrate that Hariguchi teaches "loading starting address bank run length information into a plurality of memory devices." For the foregoing reason, it is respectfully requested that the rejection of claim 41 be withdrawn.

Applicant has amended the method claims to remove the word "step" to insure that the claims are not construed as "step plus function" claims under section 112.

Applicant at this time has chosen not to address the rejection of the dependent claims as it is believed that the independent claims discussed above are in condition for allowance. Accordingly, applicant reserves the right to argue the patentability of the dependent claims should that become necessary.

Applicant has made a diligent effort to place the instant application in condition for allowance. Accordingly, a notice of allowance for claims 1-38 and 41-44 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicant's attorney at the telephone number listed below.

Respectfully submitted,



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Amendment to the Drawings:

The attached sheet of drawings includes changes to Figure 6. In Figure 6, the previously omitted label "prior art" has been added.

Attachment: Replacement Sheet

Annotated Sheet showing changes

Annotated Sheet showing changes

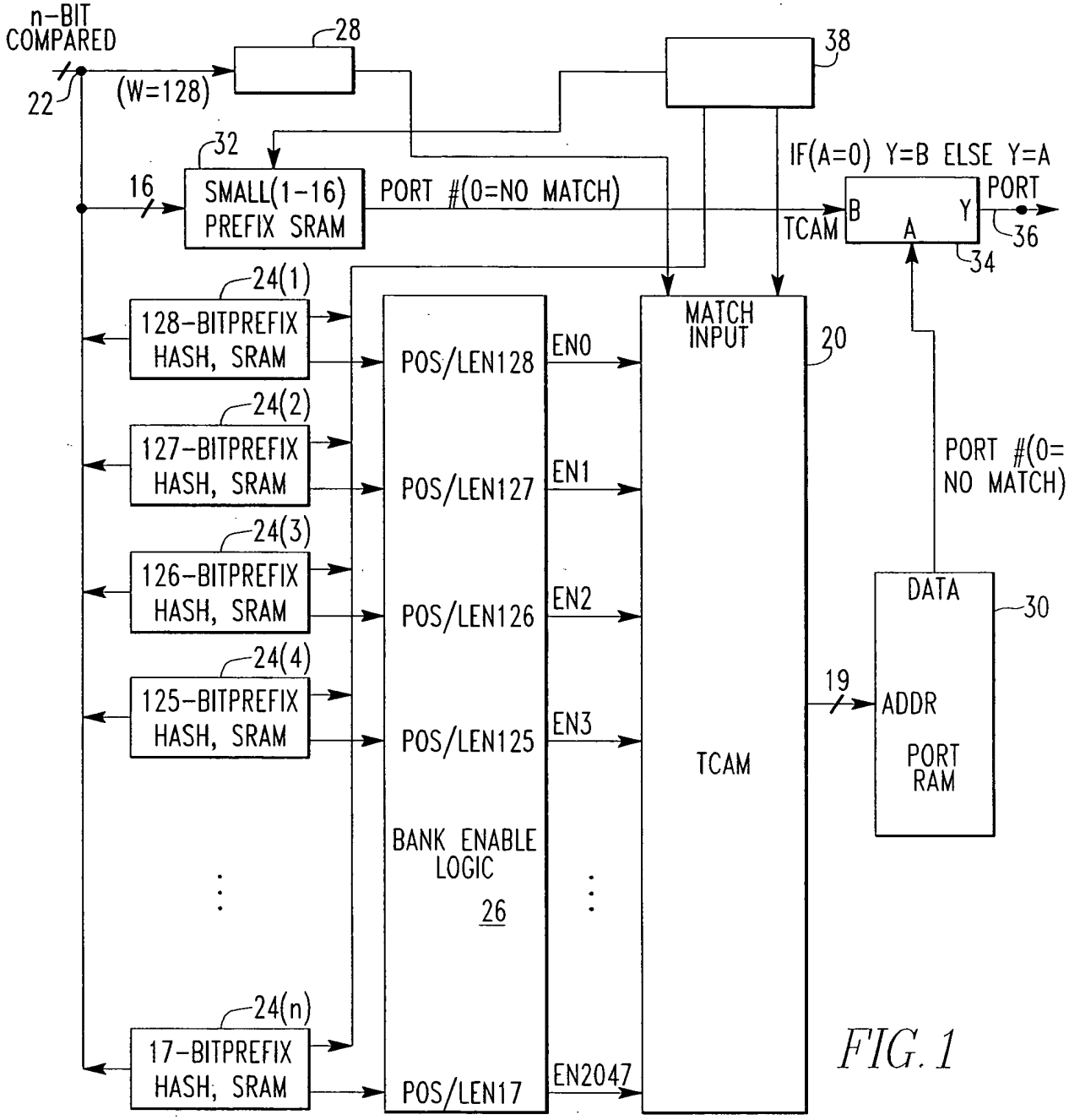

FIG. 1

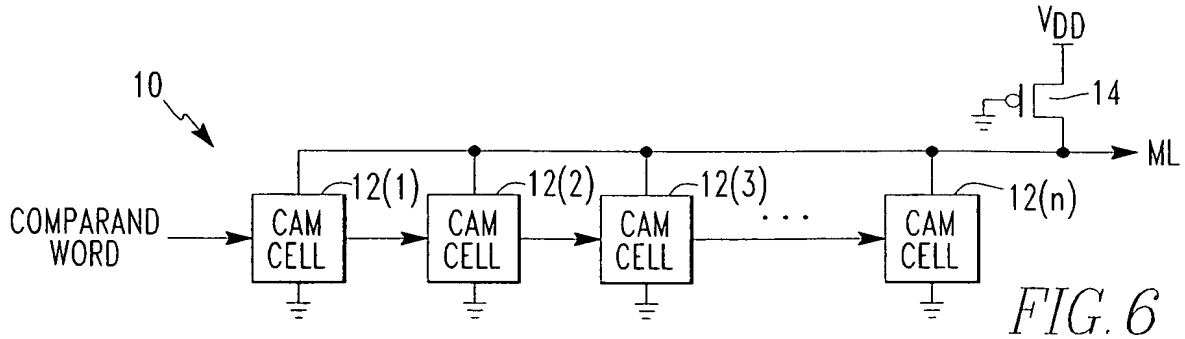

FIG. 6
PRIOR ART